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A Survey of Low Power Techniques for Efficient Network-on-Chip Design

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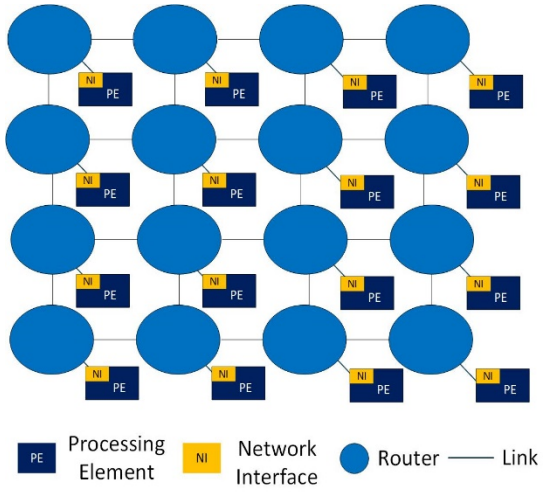
Outline

- Introduction
- Router Architecture
- Links
- NoC Architectures
- Conclusion

Introduction

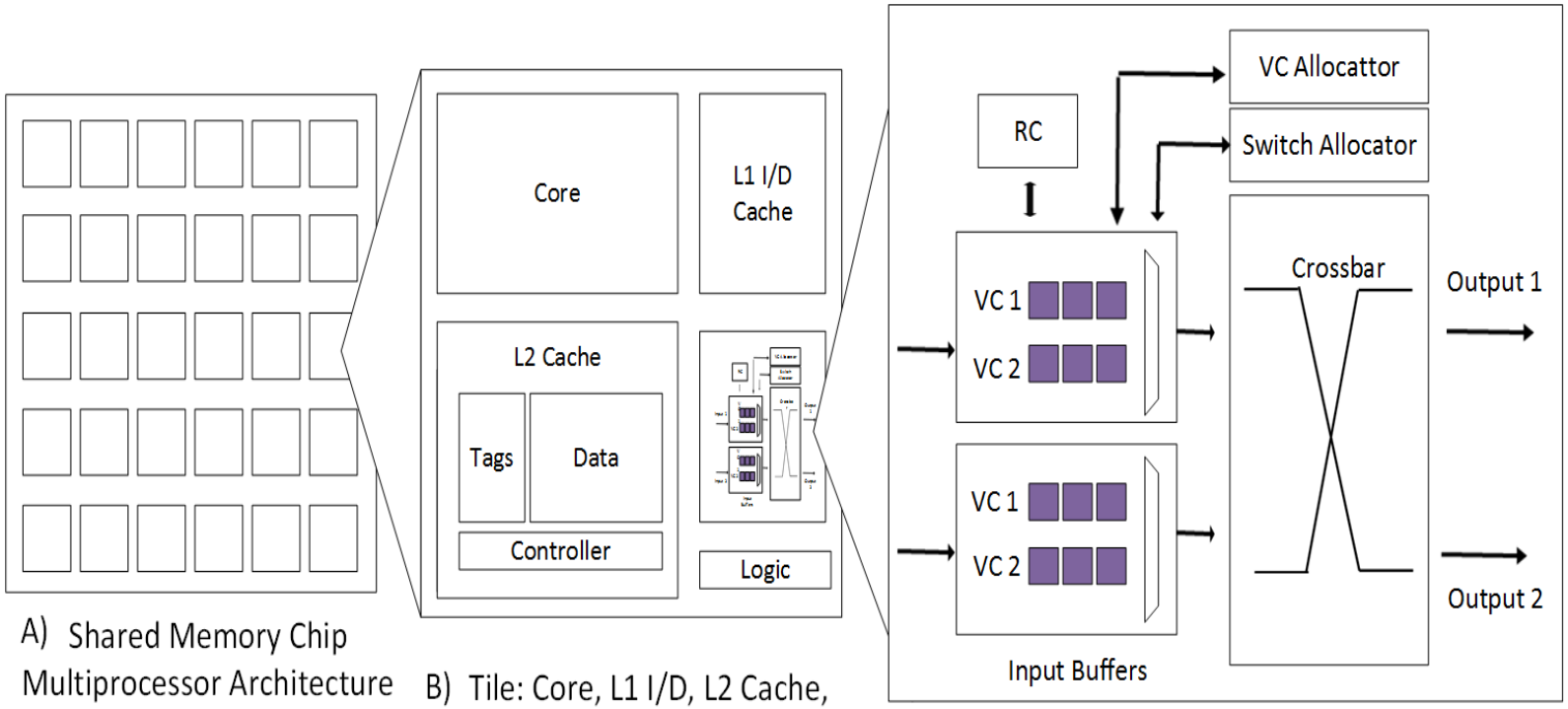
- Increase of core count limits bus-based systems from providing: High throughput, Low latency, and High bandwidth.
- The introduction of the NoC paradigm overcomes all these challenges. However, at a cost of high power consumption caused by switching activities and leakage power of the resources.



NoC router at 28nm leakage power - 40.43% of total power consumption (Hemanta Kumar Mon (2015)).

Router Architecture

Routers consist of the following elements: arbiter, buffers, virtual channels, crossbar, input and output ports. These components consume a significant amount of power.



A) Shared Memory Chip Multiprocessor Architecture

B) Tile: Core, L1 I/D, L2 Cache, Controller, Router and Logic.

C) Single-stage Router Architecture

Particularly, the input buffers consume 45% of router power and occupies 15% of area (Kundu (2006)).

A study conducted by DiTomaso (2015) reveals that 33% of dynamic power in routers are consumed by buffers.

Bufferless Routers introduced as an alternative.

Bufferless Routers

- In a bufferless router, buffers are replaced with flow control deflection algorithms, in which packets are transmitted as soon as they arrive. Therefore, the only required buffer in a bufferless router are pipeline registers.
- However, buffered routers degrade with network performance when the traffic rate increase.

Disadvantages of bufferless routers

- High Deflection rates leads to Livelock.
- Livelock leads to high power consumption.

Low Power-Techniques for Buffered Routers

- Reduction in the pipeline stages.
  - Swift NoC - The SWIFT NoC achieves low power consumption by allowing its which bypass the buffering stage to do so in one cycle; Escaping the need for read/write power. (Postman(2013))
  - Virtual circuit switching - A hybrid scheme which combines circuit and packet switching to allow flits to traverse through the network with only one stage. (Shenbagavalli(2015)).

- Power-gating techniques for NoC Router Architecture.
  - Power-gating virtual channels: Virtual Channels -Traffic-Based Virtual Channel Algorithm(S.T Muhammad(2015)), DimNoC (Zhan(2016)).

- Different type of buffers.
  - iDeal: Dual-function links (Kodi(2009)) – iDeal permits the reduction in buffer size to decrease power consumption by employing existing repeaters to function as buffers during network congestion.
  - QORE: QORE employs Multi-Function channel buffers(MFC) to be used instead of input buffers (DiTomaso(2015)).
  - The replacement of SRAM with 3T_n EDRAM to reduce buffer area by 52% and power by 43% (Li(2015)).

Crossbars

- Crossbar Size
  - The decomposition of large crossbars into smaller ones. ((Kim, 2006), (Park, 2014).
  - Multi-stage crossbars (Jiang, 2014)
- Different type of buffers.
  - The employment of packet switching and circuit switching routers. (FallahRad, 2016)

Links

- Voltage Scaling: Two working levels. Low prioritized communications can be transmitted on a low-level voltage sing while the others (Head flit) can be sent using a normal-level (A Mineo (2013)).
- Half-cycle Flits – A. Psarras et al. proposed a technique which allows flits to only use a half cycle to hop between routers. By allowing flits to spend less time in the links, less power is consumed compared to single cycle routers where one cycle is used to execute all operations in the router and one is used to hop between routers(A. Psarras(2016)).

Low Power Techniques for NoC Architectures

- Reduction in the number of TSVs in 3Ds – Monolithic 3D (D. Matos(2015)).
- RRCIES: Many cores to one router architecture (J. Fang(2015)).
- Power-gating: Sharing of resources(V. S Nandakumar).
- WiNoC: WiNoC only permits one active wireless communication. During this period, the remaining wireless interfaces which are not being used dissipate static power. Power can be reduced by in categorizing the routers in the network into three zones. These zones are high utilization zone (UTZ), low utilization zone and rare utilization zone. The routers which are rarely utilized are power-gated and have their data rerouted. As a result, 88.76% of static power in the base router can be saved (H. K Mondal(2016)).

Conclusion

- We showed
  - Power can be reduced in various NoC components.
  - Although the routers are the main area for reducing power consumption, the link and the NoC architecture itself can be optimized to save power.
- Future Work
  - Extensive evaluation and implementations have been carried out on the router architecture but not many at the link level. One of my main aims to find out more information about the links and ways in which we can optimize the power consumption.

Any Questions ?